

PATENT  
Docket No. SPLX.P0012

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Mani Adeli

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OFFICE OF PETITIONS

In re Patent Application for:

Steven Teig

Serial No.: 09/737,245

Filing Date: 12/13/00

For: METHOD AND APPARATUS FOR  
USING CONNECTION GRAPHS WITH  
POTENTIAL DIAGONAL EDGES TO MODEL  
INTERCONNECT TOPOLOGIES DURING  
PLACEMENT

Examiner: Thuan Do

Group Art Unit: 2825

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**INFORMATION DISCLOSURE  
STATEMENT UNDER 37 C.F.R. § 1.97**

Assistant Commissioner for Patents  
Washington, D.C. 20231

Dear Sir:

Pursuant to 37 C.F.R. § 1.97 and § 1.98, applicants submit for consideration in the above-identified application the documents listed on the attached Form PTO-1449. Copies of the documents are also submitted herewith. The Examiner is requested to make these documents of record.

This Information Disclosure Statement is submitted: after receipt of a first Office Action on the merits but before a final Office Action or Notice of Allowance. Applicants would

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appreciate the Examiner initialing and returning the Form PTO-1449, indicating that the information has been considered and made of record herein.

This Information Disclosure Statement under 37 C.F.R. § 1.97 is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

The requisite fee for this IDS is enclosed. In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 50-1128** referencing **SPLX.P0002**. However, the Assistant Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: March 4, 2003

Respectfully submitted,

By: \_\_\_\_\_

**Mani Adeli**

Registration No. 39,585

Stattler, Johansen & Adeli LLP

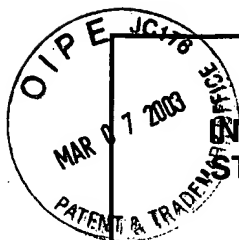
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Substitute for form 1449A/PTO <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (use as many sheets as necessary)				Application Number	09/737,245
				Filing Date	12/13/00
				First Named Inventor	Steven Teig
				Group Art Unit	2825
				Examiner Name	Thuan Do
Sheet	1	of	3	Attorney Docket Number	SPLX.P0012

U.S. PATENTS RELATED TO THE PRESENT APPLICATIONS						
Examiner* Initials	Cite No. <sup>1</sup>	U.S. Patent Document Number Kind Code <sup>2</sup> (if known)		Name of Patentee or Applicant of Cited Document	Date of Publication MM-DD-YYYY	Relation to Present Application
	1.	6,516,455	B1	Teig, et al.	02-10-02	CIP of the parent application of the present application

U.S. PATENT DOCUMENTS						
Examiner* Initials	Cite No. <sup>1</sup>	U.S. Patent Document Number Kind Code <sup>2</sup> (if known)		Name of Patentee or Applicant of Cited Document	Date of Publication MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	2.	2001/ 0003843	A1	Scepanovic et al.	06-14-01	
	3.	4,615,011		Linsker	09-30-86	
	4.	5,097,422		Corbin, II et al.	03-17-92	
	5.	5,532,934		Rostoker	07-12-96	
	6.	5,566,078		Ding et al.	10-15-96	
	7.	5,578,840		Scepanovic et al.	11-26-96	
	8.	5,634,093		Ashida et al.	05-27-97	
	9.	5,636,125		Rostoker et al.	06-03-97	
	10.	5,650,653		Rostoker et al.	07-22-97	
	11.	5,742,086		Rostoker et al.	04-21-98	
	12.	5,757,656		Hershberger et al.	05-26-98	
	13.	5,777,360		Rostoker et al.	07-07-98	
	14.	5,811,863		Rostoker et al.	09-22-98	
	15.	5,822,214		Rostoker et al.	10-13-98	
	16.	5,859,449		Kobayashi et al.	01-12-99	
	17.	5,898,597		Scepanovic et al.	04-27-99	
	18.	5,914,887		Scepanovic et al.	06-22-99	
	19.	6,035,108		Kikuchi	03-07-00	
	20.	6,058,254		Scepanovic et al.	05-02-00	

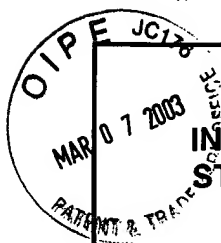
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\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Unique citation designation number. <sup>2</sup> See attached Kinds of U.S. Patent Documents. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.

<sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

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				Examiner Name	Thuan Do <b>FEB 02 2004</b>
Sheet	2	of	3	Attorney Docket Number	SPLX.P0012 <b>OFFICE OF PETITIONS</b>

U.S. PATENT DOCUMENTS						
	21.	6,068,662		Scepanovic et al.	05-30-00	
	22.	6,123,736		Pavisic et al.	09-26-00	
	23.	6,134,702		Scepanovic et al.	10-17-00	
	24.	6,155,725		Scepanovic et al.	12-05-00	
	25.	6,175,950		Scepanovic et al.	01-16-01	
	26.	6,216,252	B1	Dangelo et al.	04-10-01	
	27.	6,230,306	B1	Raspopovic et al.	05-08-01	
	28.	6,247,167	B1	Raspopovic et al.	06-12-01	
	29.	6,249,902	B1	Igusa et al.	06-19-01	
	30.	6,260,179	B1	Ohsawa et al.	07-10-01	
	31.	6,262,487	B1	Igarashi et al.	07-17-01	
	32.	6,289,495	B1	Raspopovic et al.	09-11-01	
	33.	6,301,686	B1	Kikuchi et al.	10-09-01	
	34.	6,385,758	B1	Kikuchi et al.	05-07-02	
	35.	6,401,234	B1	Alpert et al.	06-04-02	
	36.	6,405,358	B1	Nuber	06-11-02	
	37.	6,412,097	B1	Kikuchi et al.	06-25-02	
	38.	6,436,804	B2	Igarashi et al.	08-20-02	
	39.	6,463,575	B1	Takahashi	10-08-02	

FOREIGN PATENT DOCUMENTS								
Examiner* Initials	Cite No. <sup>1</sup>	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Office <sup>3</sup>	Number <sup>4</sup>	Kind Code (if known) <sup>5</sup>				
	40.	JP	64-15947		Ouchi	01-19-89		

**NON PATENT LITERATURE DOCUMENTS**

Examiner Signature		Date Considered	
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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(use as many sheets as necessary)</i>				Application Number	09/737,245	<b>RECEIVED</b>
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				Group Art Unit	2825	
				Examiner Name	Thuan Do	
Sheet	3	of	3	Attorney Docket Number	SPLX.P0012	

NON PATENT LITERATURE DOCUMENTS			
Examiner* Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>6</sup>
	41.	A.H. Farrahi et al., Quality of EDA CAD Tools: Definitions, Metrics and Directions, Quality Electronic Design, 2000, Proceedings of the first International Symposium on March 2000, pp 395-405.	
	42.	C. Chiang, et al., Wirability of Knock-Knee Layouts with 45° Wires, IEEE Transactions on Circuits and Systems, Vol. 38, Issue 6, pp 613-624, June 1991.	
	43.	G. Overtone, EDA Underwriter 2 Finding Space in a Multi-layer Board, Electronic Engineering, Morgran-Grampian LTD, vol. 67, no. 819, pp 29-30.	
	44.	J. Su et al., Post-Route Optimization for Improved Yield Using Rubber-Band Wiring Model, 1997 International Conference on Computer-Aided Design, pp 700-706, November 1997.	
	45.	J. Vicente, RSR: A New Rectilinear Steiner Minimum Tree Approximation for FPGA Placement and Global Routing, Proceedings of the 24 <sup>th</sup> Euro Micro Conference, pp 192-195, August 1998.	
	46.	K. Powers et al., The 60° Grid: Routing Channels in Width d/square root 3, VLSI, 1991, Proceedings., First Great Lakes Symposium on Kalamazoo, MI, USA, pp 214-291, March 1991.	
	47.	M. Alexander et al., Performance-Oriented Placement and Routing for field-programmable gate arrays, Proceedings of the European Design Automation Conference, pages 80-85, 1995.	
	48.	M. Alexander et al., Placement and Routing for Performance-Oriented FPGA Layout, VLSI Design, Vol. 7, No. 1, 1998.	
	49.	M. Igarashi et al., A Diagonal-Interconnect Architecture and Its Application to RISC Core Design, 2002 IEEE Solid-State Circuits Conference, pp 210-460, February 2002.	
	50.	P. Dood, et al. A Two-Dimensional Topological Compactor with Octagonal Geometry, 28 <sup>th</sup> ACM/IEEE Design Automation Conference, pp 727-731, July 1991.	
	51.	P. Parikh, et al., Congestion Driven Quadratic Placement, Proceedings of Design Automation Conference, 1998, pp 275-278.	
	52.	R. Putatunda et al., VITAL: Fully Automatic Placement Strategies for Very Large Semicustom Designs, Proceedings of the International Conference on Computer Design: VLSI in Computers and Processors, pp 434-439 October 1988.	
	53.	Y. Sekiyama et al., Timing-Oriented Routers for PCB Layout Design of High-Performance Computers, International Conference on Computer Aided Design, pp 332-335, November 1991.	

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